JÖNKÖPING UNIVERSITY
School of Engineering

COURSE SYLLABUS

Digital Electronics with VHDL, 7.5 credits

Digitalteknik med VHDL, 7.5 högskolepoäng

Course Code:	TDVK19	Education Cycle:	First-cycle level
Confirmed:	Sep 26, 2022	Disciplinary domain:	Technology
Valid From:	Jan 18, 2027	Subject group:	Computer Technology
		Specialised in:	G1F First cycle, has less than 60 credits in first-cycle course/s as entry requirements
		Main field of study:	Computer Engineering

Intended Learning Outcomes (ILO)

On completion of the course the student shall:

Knowledge and understanding

- show familiarity with time critical aspects when constructing digital circuits and find and interpret relevant data in data sheets
- show familiarity with various circuit technologies for programmable logic and how this may be combined with hard-wired cores, IP building blocks and separate microcontrollers
- display knowledge of the function of the most common data path building blocks and sequential logic circuits'
- demonstrate comprehension of the difference between asynchronous and synchronous sequential networks and how the latter may be described using Finite State Machines
- display knowledge of various digital system test- and simulation methods

Skills and abilities

- demonstrate the ability to independently design and verify modest complex digital circuits by use of VHDL
- demonstrate the ability as a member of a smaller team to design digital systems where a testbench is designed in parallel and used to verify the specification

Judgement and approach

- demonstrate the ability to choose a suitable circuit technology for implementation of a digital system

Content

The course covers digital design and a basic use of the hardware description language VHDL.

The course covers the following topics:

- The hardware description language VHDL
- Circuit technologies (e.g. CPLD, FPGA, ASIC)
- Data path building blocks (e.g. adders, multipliers)
- Sequential logic (e.g. registers, counters)
- Time critical aspects
- Finite State Machines, FSM
- Design verification (testbenches)

Type of instruction

The course consists of lectures and laboratory work.

Language of instruction is English.

Examination and grades

The course is graded 5, 4, 3 or U.

Registration of examination:

Name of the Test	Value	Grading
Examination [1]	4 credits	5/4/3/U
Laboratory work	3.5 credits	G/U

[1]Determines the final grade of the course, which is issued only when all course units have been passed.

Course literature

Please note that changes may be made to the reading list up until eight weeks before the start of the course.

Title: VHDL för konstruktion
Author: Stefan Sjöholm och Lennart Lindh (2014)
Publisher: Studentlitteratur
ISBN: 978-91-44-09373-4

Alternatively,

Title: VHDL for Designers
Author: Stefan Sjöholm and Lennart Lindh (1997)
Publisher: Prentice Hall
ISBN: 978-01-34-73414-9